Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Reset**
2. **Clock**
3. **P0**
4. **P1**
5. **P2**
6. **P3**
7. **Enable P**
8. **GND**
9. **Load**
10. **Enable T**
11. **Q3**
12. **Q2**
13. **Q1**
14. **Q0**
15. **Ripple Carry**
16. **VCC**

**.088”**

**.077”**

**3**

**4**

**5**

**6**

**2 1 16 15**

**7 8 9 10**

**14**

**13**

**12**

**11**

**NG6**

**MCHC161**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc**

**Mask Ref: MCHC161 NG6**

**APPROVED BY: DK DIE SIZE .077” X .088” DATE: 7/11/22**

**MFG: MOTOROLA THICKNESS .015” P/N: 54HC161**

**DG 10.1.2**

#### Rev B, 7/19/02